EXHIBIT E

UNITED STATES DISTRICT COURT
DISTRICT OF MASSACHUSETTS

SINGULAR COMPUTING LLC, Plaintiff, v. GOOGLE LLC, Defendant.	Civil Action No. 1:19-cv-12551-FDS Hon. F. Dennis Saylor IV

EXPERT REPORT OF SUNIL P. KHATRI, PhD.

Y=0.05% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input"

[0244] *See* § III.A.4, *supra.*

5. "wherein the number of LPHDR execution units in the device exceeds by at least one hundred the non-negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide"

[0245] *See* § III.A.7, *supra.*

IV. SINGULAR'S S1 CHIP

[0246] I have also been asked by Singular's counsel to provide my expert opinion as to whether Singular's S1 chip embodies the Asserted Claims. For the reasons explained below, I have determined that the S1 chip is an embodiment of both claim 7 of the '156 patent and claim 53 of the '273 patent.

A. Claim 7 of the '156 patent

[0247] As explained above, Claim 7 of the '156 patent depends from claim 3, which in turn depends from claim 2, which itself depends from independent claim 1. In § III.A above, I include the language of claim 7 written in independent form, incorporating all of the limitations of its parent claims.

[0248] Based on my review of the evidence and my professional experience and expertise, the S1 chip comprises "at least one first low precision high-dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value."

[0249] For example, the S1 has at least one approximate processing element (APE) and has an array of execution units. *See* SINGULAR-00009701 at 9703. The APEs receive signals representing values and performs operations on those signals, including arithmetic operations. *See id.* at 00009701-4. Each processing element has an arithmetic logic unit (ALU) that, given two values, can add, subtract, multiply, and divide the values, and given one value, can compute its square root. *See id.* at 00009708.

[0250] Based on my review of the evidence and my professional experience and expertise, the S1 chip meets the requirement that "the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000."

[0251] In the S1, the dynamic range of possible valid inputs is from approximately 10^{-19} to 10^{19}. *See* SINGULAR-00014320 at 14329.

[0252] Based on my review of the evidence and my professional experience and expertise, the S1 chip satisfies the requirement of claim 7 that "for at least X=5% of the possible valid inputs to the first operating, the statistical mean, over repeated execution of the first operating on each specific input from the at least X% of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.05% from the result of an exact mathematical calculation of the first operating on the numerical values of that same input."

[0253] For example, I understand that tests involving the S1 established that approximately 50% of valid inputs sent to an APE produced an output error exceeding 0.2% for at least the square root operation. *See* SINGULAR-00027686.

[0254] Based on my review of the evidence and my professional experience and expertise, the S1 chip also comprises "at least one first computing device adapted to control the operation of the at least one first LPHDR execution." By way of example, the S1 chip includes a control unit (CU) that is adapted to control the operation of the APEs. *See* SINGULAR-00014320 at 14322.

[0255] Based on my review of the evidence and my professional experience and expertise, the S1 chip also satisfies the requirement that "the at least one first computing device comprises at least one of a central processing unit (CPU), a graphics processing unit (GPU), a field programmable gate array (FPGA), a microcode-based processor, a hardware sequencer, and a state machine."

[0256] For example, the S1 comprises a Xilinx Zynq device, which comprises a dual core ARM processor and an FPGA. *See* SINGULAR-00014320 at 14322. The ARM processor is the S1 CPU and the FPGA is programmed to be the S1 Control Unit. *See* SINGULAR-00009701 at 9703.

[0257] Based on my review of the evidence and my professional experience and expertise, the S1 chip also satisfies the requirement of claim 7 that "the number of LPHDR execution units in the device exceeds by at least one hundred the non-negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating pint numbers that are at least 32 bits wide."

[0258] In the S1, there are at least 2,000 APEs. *See* SINGULAR-00009701 at 9704. Indeed, in some configurations, there is an array of 16 ASICs each of which contains over 2,000 APEs, (containing more than 32,000 APEs in total). *Id.*. By contrast, every configuration of the S1 chip comprises only "approximate" "Singular-style" floating point multipliers. *See* SINGULAR-00009701.The Xilinx Zynq device used in the S1 has two ARM cores, each of which has single and double precision floating point units which include a multiplier. *See* SINGULAR-00009701 at 03; *see also* Zynq-7000 SoC Data Sheet: Overview.[13] This makes for a total of at most 4 32-bit or higher floating point multipliers. Therefore, in every configuration, the number of LPHDR execution units in the S1 chip exceeds the number of of 32-bit multipliers by more than 100.

B. Claim 53 of the '273 patent

[0259] As I explained above, claim 53 of the '273 patent depends from claim 43, which in turn depends from independent claim 36. In § III.B above, I include the language of claim 53 written in independent form, incorporating all of the limitations of its parent claims.

[0260] As I explain in § III.B above, it is evident that every limitation of claim 53 of the '273 patent is also recited verbatim in claim 7 of the '156 patent. Accordingly, in my opinion, the S1 chip meets all the limitations of claim 53 of the '273 patent for at least the reasons given in § IV.A above.

[13] Available at https://www.mouser.com/datasheet/2/903/ds190-Zynq-7000-Overview-1595492.pdf (Attached as **Exhibit K**).

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Date: December 22, 2022.

Sunil P Khatri, Ph.D.